Five-Level Inverter for Renewable Power Generation System

Jia-Min Shen, *Member, IEEE*, Hurng-Liahng Jou, *Member, IEEE*, Jinn-Chang Wu, *Member, IEEE*, and Kuen-Der Wu

***Abstract*—In this paper, a five-level inverter is developed and applied for injecting the real power of the renewable power into the grid to reduce the switching power loss, harmonic distortion, and electromagnetic interference caused by the switching operation of power electronic devices. Two dc capacitors, a dual-buck converter, a full-bridge inverter, and a filter configure the five-level inverter. The input of the dual-buck converter is two dc capacitor voltage sources. The dual-buck converter converts two dc capacitor voltage sources to a dc output voltage with three levels and balances these two dc capacitor voltages. The output voltage of the dual-buck converter supplies to the full-bridge inverter. The power electronic switches of the full-bridge inverter are switched in low frequency synchronous with the utility voltage to convert the output voltage of the dual-buck converter to a five-level ac voltage. The output current of the five-level inverter is controlled to generate a sinusoidal current in phase with the utility voltage to inject into the grid. A hardware prototype is developed to verify the performance of the developed renewable power generation system. The experimental results show that the developed renewable power generation system reaches the expected performance.**

***Index Terms*—Harmonic distortion, inverters, power electronics.**

I. Introduction

THE conventional single-phase inverter topologies for grid-connection include half-bridge and full bridge [1]–[4]. The half-bridge inverter is configured by one capacitor arm and one power electronic arm. The dc bus voltage of the half-bridge inverter must be higher than double of the peak voltage of the output ac voltage. The output ac voltage of the half-bridge inverter is two levels. The voltage jump of each switching is the dc bus voltage of the inverter. The full-bridge inverter is configured by two power electronic arms. The popular modulation strategies for the full-bridge inverter are bipolar modulation and unipolar modulation [3], [5]–[7]. The dc bus voltage of the full-bridge inverter must be higher than the peak voltage of the output ac voltage. The output ac voltage of the full-bridge inverter is two levels if the bipolar modulation is used and three levels if the unipolar modulation is used. The voltage jump of each switching is double the dc bus voltage of the inverter if the bipolar modulation is used, and it is the dc bus voltage of the inverter if the unipolar modulation is used. All power electronic switches operate in high switching frequency in both half-bridge and full-bridge inverters. The switching operation will result in switching loss. The loss of power electronic switch includes the switching loss and the conduction loss. The conduction loss depends on the handling power of power electronic switch. The switching loss is proportional to the switching frequency, voltage jump of each switching, and the current of the power electronic switches. The power efficiency can be advanced if the switching loss of the dc–ac inverter is reduced.

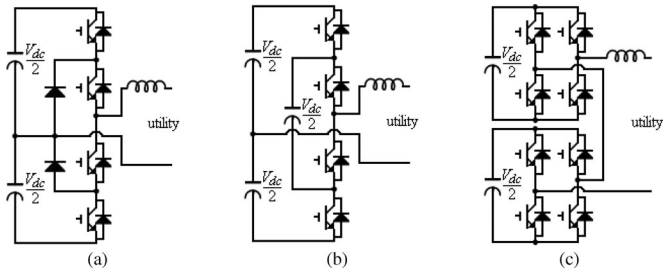

Fig. 1. Circuit configuration of conventional single-phase multilevel inverter. (a) Diode clamped. (b) Flying capacitor. (c) Cascade H-bridge.

Multilevel inverter can effectively reduce the voltage jump of each switching operation to reduce the switching loss and increase power efficiency. The number of power electronic switches used in the multilevel inverter is larger than that used in the conventional half-bridge and full-bridge inverters. Moreover, its control circuit is more complicated. Thus, both the performance and complexity should be considered in designing the multilevel inverter [8], [9]. However, interest in the multilevel inverter has been aroused due to its advantages of better power efficiency, lower switching harmonics, and a smaller filter inductor compared with the conventional half-bridge and full-bridge inverters.

The conventional single-phase multilevel inverter topologies include the diode-clamped, the flying capacitor, and the cascade H-bridge types [10]–[15], as shown in Fig. 1. Fig. 1(a) shows the basic configuration of a diode-clamped multilevel inverter. As can be seen, it is configured by two dc capacitors, two diodes, and four power electronic switches. Two diodes are used to conduct the current loop, and four power electronic switches are used to control the voltage levels. The output voltage of the basic diode-clamped multilevel inverter has three levels. The voltage difference of each level is $V_{\rm dc}/2$ (the voltage on a capacitor). Since the voltages of two dc capacitors are used to form the voltage level of the multilevel inverter, the voltages of these two dc capacitors must be controlled to be equal. The control for balancing these two dc capacitors is very important

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in controlling the diode-clamped multilevel inverter, and it is very hard under the light load [16]–[19]. If the five-level output voltage is expected, extra two diodes and four power electronic switches are required [11], [20]. Fig. 1(b) shows the circuit configuration of a basic flying capacitor multilevel inverter. As can be seen, it is configured by three dc capacitors and four power electronic switches. The voltage on each dc capacitor is controlled to be $V_{\rm dc}/2$, and the output voltage of the basic flying capacitor multilevel inverter has three levels. The voltage difference of each level is also $V_{\rm dc}/2$ (the voltage on a dc capacitor). These three dc capacitors must be controlled for maintaining their voltages to be $V_{\rm dc}/2$ in the charge and discharge processes. Therefore, its control circuit is more complicated. If five-level output voltage is required, an extra dc capacitor and four power electronic switches are required [11], [13], [14]. Fig. 1(c) shows the circuit configuration of the basic cascade H-bridge multilevel inverter [8]–[11], [15], [21]. As can be seen, it is configured by two full-bridge inverters connected in cascade. The dc bus voltage of each full-bridge inverter is $V_{\rm dc}/2$, and the output voltage of each full-bridge inverter can be controlled to be $V_{\rm dc}/2$, 0, and $-V_{\rm dc}/2$. Thus, the voltage levels of the output voltage of the cascade full-bridge multilevel inverter are $V_{\rm dc}$, $V_{\rm dc}/2$, 0, $-V_{\rm dc}/2$, and $-V_{\rm dc}$. This topology has advantages of fewer components being required compared with other multilevel inverters under the output voltage with the same levels, and its hardware circuit can be modularized because the configuration of each full bridge is the same. However, this topology has the disadvantages that two independent dc voltage sources are required.

In this paper, a five-level inverter is developed and applied for injecting the real power of the renewable power into the grid. This five-level inverter is configured by two dc capacitors, a dual-buck converter, a full-bridge inverter, and a filter [22]. The five-level inverter generates an output voltage with five levels and applies in the output stage of the renewable power generation system to generate a sinusoidal current in phase with the utility voltage to inject into the grid. The power electronic switches of the dual-buck converter are switched in high frequency to generate a three-level voltage and balance the two input dc voltages. The power electronic switches of the full-bridge inverter are switched in low frequency synchronous with the utility to convert the output voltage of the dual-buck converter to a five-level ac voltage. Therefore, the switching power loss, harmonic distortion, and electromagnetic interference (EMI) caused by the switching operation of power electronic devices can be reduced, and the control circuit is simplified. Besides, the capacity of output filter can be reduced. A hardware prototype is developed to verify the performance of the developed renewable power generation system.

II. Circuit Configuration

Fig. 2 shows the circuit configuration of the five-level inverter applied to a photovoltaic power generation system. As can be seen, it is configured by a solar cell array, a dc–dc converter, a five-level inverter, two switches, and a digital signal processor (DSP)-based controller. Switches SW_1 and SW_2 are placed between the five-level inverter and the utility, and they are used to disconnect the photovoltaic power generation system from the utility when islanding operation occurs. The load is placed between switches SW_1 and SW_2. The output of the solar cell array is connected to the input port of the dc–dc converter. The output port of the dc–dc converter is connected to the five-level inverter. The dc–dc converter is a boost converter, and it performs the functions of maximum power point tracking (MPPT) and boosting the output voltage of the solar cell array. This five-level inverter is configured by two dc capacitors, a dual-buck converter, a full-bridge inverter, and a filter. The dual-buck converter is configured by two buck converters. The two dc capacitors perform as energy buffers between the dc–dc converter and the five-level inverter. The output of the dual-buck converter is connected to the full-bridge inverter to convert the dc voltage to ac voltage. An inductor is placed at the output of the full-bridge inverter to form as a filter inductor for filtering out the high-frequency switching harmonic generated by the dual-buck converter.

III. Operation Principle of Five-Level Inverter

The operation of this five-level inverter can be divided into eight modes. Modes 1–4 are for the positive half-cycle, and modes 5–8 are for the negative half-cycle. Fig. 3 shows the operation modes of five-level inverter. As can be seen, the power electronic switches of the full-bridge inverter are switched in low frequency and synchronously with the utility voltage to convert the dc power into ac power for commutating. As seen in Fig. 3(a)–(d), the power electronic switches S_4 and S_7 are in the ON state, and the power electronic switches S_5 and S_6 are in the OFF state during the positive half-cycle. On the contrary, the power electronic switches S_4 and S_7 are in the OFF state, and the power electronic switches S_5 and S_6 are in the ON state during the negative half-cycle. Since the dc capacitor voltages V_{C2} and V_{C3} are balanced by controlling the five-level inverter, the dc capacitor voltages V_{C2} and V_{C3} can be represented as follows:

$$V_{C2} = V_{C3} = \frac{1}{2}V_{\rm dc}. \tag{1}$$

The operation modes of this five-level inverter are stated as follows.

Mode 1: Fig. 3(a) shows the operation circuit of mode 1. The power electronic switch of the dual-buck converter S_2 is turned ON and S_3 is turned OFF. DC capacitor C_2 is discharged through S_2, S_4, the filter inductor, the utility, S_7, and D_3 to form a loop. Both output voltages of the dual-buck converter and five-level inverter are $V_{\rm dc}/2$.

Mode 2: Fig. 3(b) shows the operation circuit of mode 2. The power electronic switch of the dual-buck converter S_2 is turned OFF and S_3 is turned ON. DC capacitor C_3 is discharged through D_2, S_4, the filter inductor, the utility, S_7, and S_3 to form a loop. Both output voltages of the dual-buck converter and five-level inverter are $V_{\rm dc}/2$.

Mode 3: Fig. 3(c) shows the operation circuit of mode 3. Both power electronic switches S_2 and S_3 of the dual-buck converter

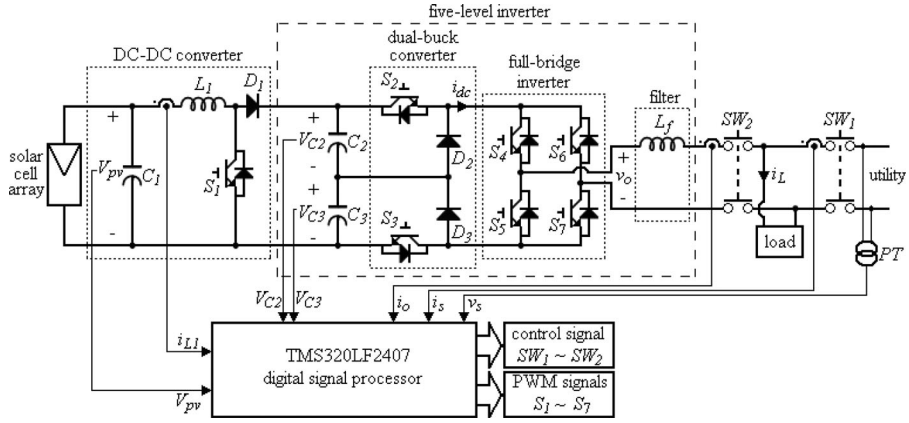

Fig. 2. Circuit configuration of the developed photovoltaic power generation system.

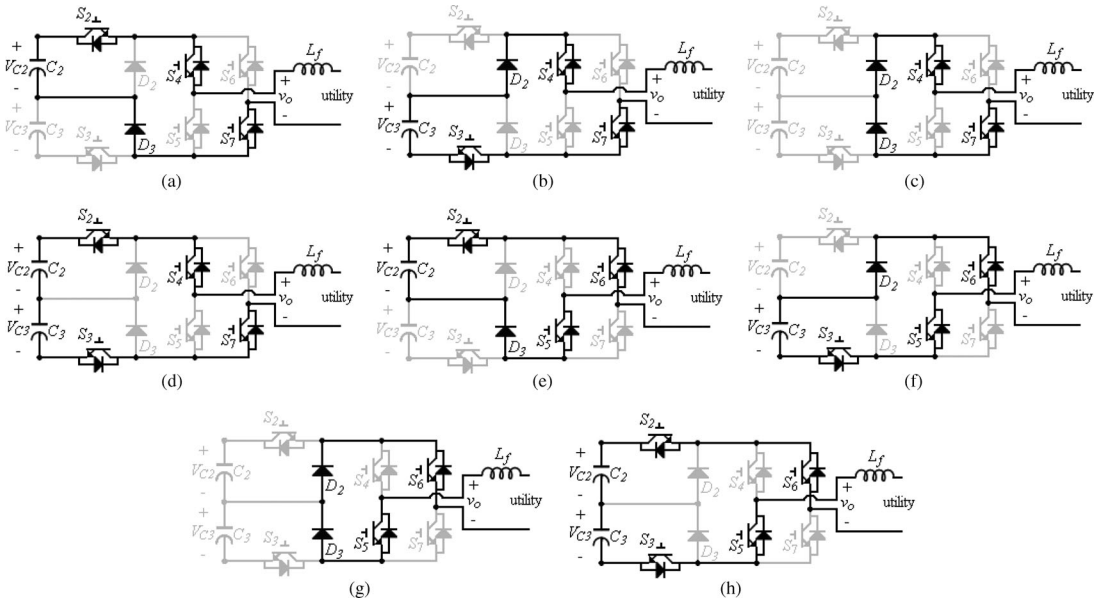

Fig. 3. Operation modes of the five-level inverter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8.

are turned OFF. The current of the filter inductor flows through the utility, S_7, D_3, D_2, and S_4. Both output voltages of the dual-buck converter and five-level inverter are 0.

Mode 4: Fig. 3(d) shows the operation circuit of mode 4. Both power electronic switches S_2 and S_3 of the dual-buck converter are turned ON. DC capacitors C_2 and C_3 are discharged together through S_2, S_4, the filter inductor, the utility, S_7, and S_3 to form a loop. Both output voltages of the dual-buck converter and five-level inverter are $V_{\rm dc}$.

Modes 5–8 are the operation modes for the negative half-cycle. The operations of the dual-buck converter under modes 5–8 are similar to that under modes 1–4, and the dual-buck converter can also generate three voltage levels $V_{\rm dc}/2$, $V_{\rm dc}/2$, 0, and $V_{\rm dc}$, respectively. However, the operation of the full-bridge inverter is the opposite. The power electronic switches S_4 and S_7 are in the OFF state, and the power electronic switches S_5 and S_6 are in the ON state during the negative half-cycle. Therefore, the output voltage of the five-level inverter for modes 5–8 will be $-V_{\rm dc}/2$, $-V_{\rm dc}/2$, 0, and $-V_{\rm dc}$, respectively.

Considering operation modes 1–8, the full-bridge inverter converts the dc output voltage of the dual-buck converter with three levels to an ac output voltage with five levels which are $V_{\rm dc}$, $V_{\rm dc}/2$, 0, $-V_{\rm dc}/2$, and $-V_{\rm dc}$.

The operation of power electronic switches S_2 and S_3 should guarantee the output voltage of the dual-buck converter is higher than the absolute of the utility voltage. The waveforms of output voltage of five-level inverter and utility voltage are shown in Fig. 4.

Due to the operation of full-bridge inverter, the voltage and current in the dc side of full-bridge inverter are their absolute values of the utility voltage and the output current of the five-level inverter. When the absolute of the utility voltage is smaller than $V_{\rm dc}/2$, the output voltage of the dual-buck converter should change between $V_{\rm dc}/2$ and 0. Accordingly, the power electronics of five-level inverter is switched between modes 1 or 2, and mode 3 during the positive half-cycle. On the contrary, the power electronics of five-level inverter is switched between modes 5 or 6, and mode 7 during the negative half-cycle. One of the power

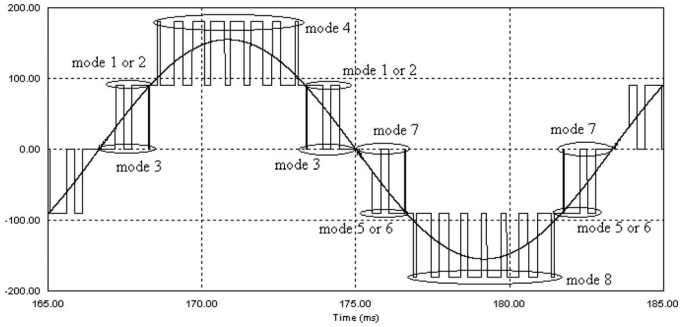

Fig. 4. Waveforms of output voltage and utility voltage.

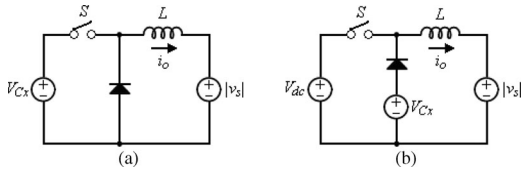

Fig. 5. Equivalent circuit. (a) $|v_s| < V_{\rm dc}/2$. (b) $|v_s| > V_{\rm dc}/2$.

electronic switches S_2 and S_3 is in the OFF state and the other is switched in high frequency during one PWM period. Fig. 5(a) shows the equivalent circuit for the dc side of the five-level inverter under $|v_s| < V_{\rm dc}/2$. As seen in Fig. 5(a), the equivalent circuit is a conventional buck converter. DC voltage source V_{cx} may be dc capacitor voltage V_{C2} or V_{C3}, and it depends on which power electronic switch S_2 or S_3 is switching in high frequency. As the power electronic switch is turned ON, the change rate of the output current can be represented as follows:

$$\frac{d\,|i_o|}{dt} = \frac{V_{Cx} - |v_s|}{L} \tag{2}$$

where L is the inductance of the filter inductor. The change rate of the output current is positive. Thus, the output current $|i_o|$ increases when the power electronic switch is turned ON. As the power electronic switch is turned OFF, the change rate of the output current can be represented as follows:

$$\frac{d\,|i_o|}{dt} = \frac{-|v_s|}{L}. \tag{3}$$

The change rate of the output current is negative, meaning the output current $|i_o|$ will decrease when the power electronic switch is turned OFF. As seen in (2) and (3), the output current $|i_o|$ can be controlled by controlling the ON/OFF operation of the power electronic switch to track a reference current signal.

When the absolute of the utility voltage is higher than $V_{\rm dc}/2$, the output voltage of the dual-buck converter should be changed between $V_{\rm dc}$ and $V_{\rm dc}/2$. Accordingly, the five-level inverter is operated in mode 4, and 1 or 2 during the positive half-cycle, and it is switched in mode 8, and 5 or 6 during the negative half-cycle. One of power electronic switches S_2 and S_3 is still turned ON and the other is switched in high frequency during one PWM period. Fig. 5(b) shows the equivalent circuit for the dc side of the five-level inverter under $|v_s| > V_{\rm dc}/2$. The dc voltage source $V_{\rm dc}$ is the summation of dc capacitor voltages V_{C2} and V_{C3}. As seen in Fig. 5(b), it differs from the conventional buck converter, where voltage source V_{Cx} is connected to the diode in series. Voltage source V_{cx} may be dc capacitor voltage V_{C2} or V_{C3}, and it depends on which power electronic switch S_3 or S_2 is switching in high frequency. As the power electronic switch is turned ON, the change rate of the output current can be represented as follows:

$$\frac{d\,|i_o|}{dt} = \frac{V_{\rm dc} - |v_s|}{L}. \tag{4}$$

The change rate of the output current $|i_o|$ is positive, meaning the output current $|i_o|$ increases when the power electronic switch is turned ON. As the power electronic switch is turned OFF, the change rate of the output current can be represented as follows:

$$\frac{d\,|i_o|}{dt} = \frac{V_{Cx} - |v_s|}{L}. \tag{5}$$

The change rate of the output current $|i_o|$ is negative, and the output current $|i_o|$ inductor current will be decreased when the power electronic switch is turned OFF. As seen in (4) and (5), the output current $|i_o|$ can also be controlled to track a reference current signal by controlling the ON/OFF operation of the power electronic switches under $|v_s| > V_{\rm dc}/2$.

Hence, the output current of the five-level inverter can be controlled to track a reference current signal, which is a sinusoidal current in phase with the utility voltage by controlling the ON/OFF operation of the power electronic switches S_2 and S_3. Meanwhile, the five-level inverter will generate a five-level output voltage varying with the change of the utility voltage. The switching loss, filter inductor, and EMI are reduced because the voltage difference of each voltage level is only $V_{\rm dc}/2$.

IV. Voltage Balance of Five-Level Inverter

Balancing the voltages of dc capacitors is very important in controlling the multilevel inverter. The voltage balance of dc capacitor voltages V_{C2} and V_{C3} can be controlled by the power electronic switches S_2 and S_3 easily. When the absolute of the utility voltage is smaller than $V_{\rm dc}/2$, one power electronic switch either S_2 or S_3 is switched in high frequency and the other is still in the OFF state. Which power electronic switch is switched in high frequency depends on the dc capacitor voltages V_{C2} and V_{C3}. If dc capacitor voltage V_{C2} is higher than dc capacitor voltage V_{C3}, power electronic switch S_2 is switched in high frequency. In this situation, the voltage source V_{Cx} in Fig. 5(a) is V_{C2}, and C_2 will be discharged. Thus, the dc capacitor voltages V_{C2} decreases and V_{C3} does not change. On the contrary, power electronic switch S_3 is switched in high frequency when voltage V_{C3} is higher than voltage V_{C2}. In this situation, the voltage source V_{Cx} in Fig. 5(a) is V_{C3}. Thus, the dc capacitor voltages V_{C3} decreases and V_{C2} does not change. In this way, the voltage balance of C_2 and C_3 can be achieved.

When the absolute of the utility voltage is higher than $V_{\rm dc}/2$, one power electronic switch either S_2 or S_3 is switched in high frequency and the other is still in the ON state. Which power electronic switch is switched in high frequency depends on the dc capacitor voltages V_{C2} and V_{C3}. If dc capacitor voltage V_{C2} is higher than dc capacitor voltage V_{C3}, the power electronic switch S_3 is switched in high frequency. The voltage source V_{Cx}

TABLE I
ON/OFF STATE OF S_2 AND S_3

		$\|v_s\|<V_{dc}/2$	$\|v_s\|>V_{dc}/2$
$V_{C2}>V_{C3}$	S_2	PWM	on
	S_3	off	PWM
$V_{C2}<V_{C3}$	S_2	off	PWM
	S_3	PWM	on

in Fig. 5(b) is dc capacitor voltage V_{C2}. When the power electronic switch S_3 is turned ON, both C_2 and C_3 are discharged. However, only C_2 supplies the power when the power electronic switch S_3 is turned OFF. Thus, C_2 will discharge more power than that of C_3. On the contrary, the power electronic switch S_2 is switched in high frequency when dc capacitor voltage V_{C3} is higher than dc capacitor voltage V_{C2}. The voltage source V_{Cx} in Fig. 5(b) is dc capacitor voltage V_{C3}. When the power electronic switch S_2 is turned ON, both C_2 and C_3 are discharged. However, only C_3 supplies the power when the power electronic switch S_2 is turned OFF. Thus, C_3 will discharge more power than that of C_2. In this way, the voltage balance of C_2 and C_3 can be achieved.

As mentioned earlier, the operation of power electronic switches S_2 and S_3 can be summarized as Table I. The voltages of capacitors C_2 and C_3 can be easily balanced compared with the conventional multilevel inverter.

V. CONTROL BLOCK DIAGRAM

The developed photovoltaic power generation system consists of a dc–dc power converter and the five-level inverter. The five-level inverter performs the functions of converting the dc power into high-quality ac power and injecting it into the utility, balancing two dc capacitor voltages V_{C2} and V_{C3}, and detecting the islanding operation. The dc–dc converter boosts the output voltage of the solar cell array and performs the MPPT to extract the maximum output power of the solar cell array. The controllers of both the dc–dc converter and the five-level inverter are explained as follows.

A. Five-Level Inverter

Fig. 6 shows the control block diagram of five-level inverter. In the operation of the five-level inverter, the dc bus voltage must be regulated to be larger than the peak voltage of the utility, and the dc capacitor voltages of C_2 and C_3 must be controlled to be equal. Besides, the five-level inverter must generate a sinusoidal current in phase with the utility voltage to be injected into the utility. As seen in Fig. 6, the voltages of dc capacitors C_2 and C_3 are detected and then added to obtain a dc bus voltage $V_{\rm dc}$. The added result is subtracted from a dc bus setting voltage V_dc_set. The dc bus setting voltage V_dc_set is larger than the peak voltage of the utility. The subtracted result is sent to a P-I controller.

An islanding detection is also incorporated into the control of the five-level inverter. The concept of this islanding detection was proposed by authors [23]. However, it will not be addressed in this paper.

As seen in Fig. 6, the utility current is detected and sent to an RMS detection circuit. The output of the RMS detection circuit is sent to a hysteresis comparator that contains a low threshold value and a high threshold value. If the RMS value of the utility current is smaller than the low threshold value, the output of the hysteresis comparator is high, meaning the condition of islanding operation or power balance occurs. On the contrary, the output of the hysteresis comparator is low when the RMS value of the utility current is larger than the high threshold value, meaning the utility is normal. The output of the hysteresis comparator is sent to a signal generator. The output signal of the signal generator is an islanding control signal S_a. The islanding control signal is a dc signal with unity amplitude if the output of the hysteresis comparator is low. On the contrary, the islanding control signal is a square wave with a frequency of 20 Hz (disturbance signal for islanding detection) when the output of the hysteresis comparator is high. The outputs of the P-I controller and signal generator are sent to a multiplier, and the product of the multiplier is the amplitude of the reference signal. The utility voltage is detected and then sent to a phase-lock loop (PLL) circuit to generate an unity-amplitude sinusoidal signal whose phase is in phase with the utility voltage. The outputs of the multiplier and the PLL circuit are sent to the other multiplier. The product of this multiplier is the reference signal of the output current for the five-level inverter. The output current of the five-level inverter is detected by a current sensor. The reference signal and detected signal for the output current of the five-level inverter are sent to a subtractor. The subtracted result is sent to a current-mode controller. The output of the current-mode controller is sent to a PWM circuit to generate a PWM signal. The detected dc capacitor voltages V_{C2} and V_{C3} are also sent to a comparator to obtain signal S_b. When dc capacitor voltage V_{C2} is higher than dc capacitor voltage V_{C3}, S_b is a high value. On the contrary, S_b is a low value when dc capacitor voltage V_{C2} is smaller than dc capacitor voltage V_{C3}. DC voltage $V_{\rm dc}$ is also sent to an amplifier with a gain of 0.5 to obtain voltage signal $V_{\rm dc}/2$. The detected utility voltage is sent to an absolute circuit to obtain voltage signal $|v_s|$. Voltage signals $V_{\rm dc}/2$ and $|v_s|$ are compared to obtain signal S_c. When $V_{\rm dc}/2 > |v_s|$, S_c is a high value. On the contrary, S_c is a low value when $V_{\rm dc}/2 < |v_s|$. The output signal of the PWM circuit and signals S_b and S_c are sent to the mode selection circuit. The output of the mode selection circuit will generate the control signals of power electronic switches S_2 and S_3 according to Table I. The detected utility voltage is also sent to a comparator to obtain complementary square signals that are synchronous with the detected utility voltage. The complementary square signals are the control signals of the power electronic switches of the full-bridge inverter. As mentioned earlier, only two power electronic switches S_2 or S_3 in the five-level inverter should be switched in high frequency, and only one of them is switched in high frequency at any time, and the voltage level of every switching is $V_{\rm dc}/2$. Therefore, the five-level inverter can reduce the switching loss effectively.

B. DC–DC Converter

Fig. 7 shows the control block of the dc–dc converter. The input of the dc–dc converter is the output of the solar cell array.

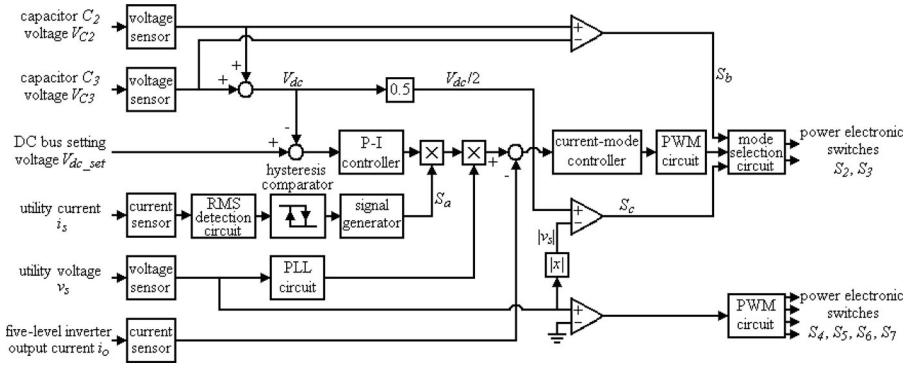

Fig. 6. Control block diagram of five-level inverter.

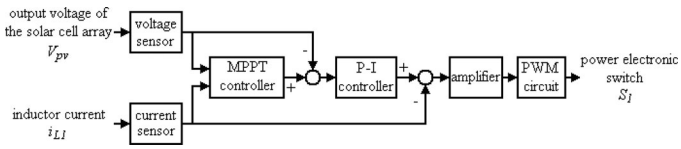

Fig. 7. Control block of the dc–dc converter.

A ripple voltage with a frequency double that of the utility will appear in the dc bus voltage $V_{\rm dc}$, while the five-level inverter injects real power into the utility. The function of MPPT will be degraded, while the output voltage of solar cell array contains a ripple voltage. Therefore, the ripple voltage superimposed on the dc bus voltage $V_{\rm dc}$ must be blocked by the dc–dc converter for improving the function of MPPT. Accordingly, the dual control loops, an outer voltage control loop, and an inner current control loop are applied to control the dc–dc converter. Since the output voltage of the dc–dc converter is the dc bus voltage that is controlled to be a constant voltage by the five-level inverter, the outer voltage control loop is used to regulate the output voltage of the solar cell array. The inner current control loop is applied to control the inductor current to approach a constant current to block the ripple voltage of dc bus voltage $V_{\rm dc}$. The perturbation and observation method is adopted to obtain the function of MPPT [24], and it is incorporated into the controller of the dc–dc converter. The output of the MPPT controller is the desired output voltage of the solar cell array, and it is the reference voltage of the outer voltage control loop. The output voltage of the solar cell array is perturbed first, and then the output power variation of the solar cell array is observed to determine the next perturbation for the output voltage of the solar cell array. The output power of the solar cell array is calculated from the product of the output voltage of the solar cell array and the inductor current. Therefore, the output voltage of the solar cell array and the inductor current are detected and sent to a MPPT controller to determine the desired output voltage of the solar cell array. The detected output voltage and desired output voltage of the solar cell array are sent to a subtractor, and the subtracted result is sent to a P-I controller. The output of the P-I controller is the reference signal of the inner current control loop. The reference signal and the detected inductor current are sent to a subtractor, and the subtracted result is sent to an amplifier to complete the inner current control loop. The output of the amplifier is sent to the PWM circuit. The output signal of the PWM circuit is the driving signal for the power electronic switch of the dc–dc converter.

TABLE II
MAJOR PARAMETERS USED IN THE EXPERIMENTS

Solar module	
Rate of maximum power	75W
Open voltage	21.7V
Short current	5.0A
DC-DC converter	
Capacitor (C_1)	470μF
Inductor (L_1)	2mH
Switch frequency	20kHz
Five-level inverter	
DC bus capacitor (C_2 and C_3)	2,200μF
Filter inductor (L_f)	1.4mH
DC bus setting voltage	170V
Switch frequency (PWM)	20kHz
Utility voltage	110V
Utility frequency	60Hz

For protecting the renewable power generation system from the voltage rise, the MPPT function will be disabled and the power electronic switch S_1 will be turned OFF when the inverter stage is interrupted after detecting the islanding operation. Therefore, the output voltage of solar cell array is limited to the open-circuit voltage of solar cell array, and the dc bus voltage $V_{\rm dc}$ is also limited.

VI. EXPERIMENTAL RESULTS

To verify the performance of the photovoltaic power generation system using the five-level inverter, a prototype based on the DSP controller of TMS320LF2407 A is developed and tested. The main parameters of the prototype are listed in Table II. The solar cell array consists of two strings, and each string contains eight solar modules connected in series. The capacity of solar cell array is 1.2 kW.

Fig. 8 shows the experimental results for the characteristics of the solar cell array. The environmental temperature and radiation levels are 30.7 °C and 922 W/m^2, respectively. The temperature of the solar module is 52.3 °C. The maximum output power of the solar cell array is about 830 W. Fig. 9 shows the experimental results of MPPT performance for the developed photovoltaic power generation system. The MPPT controller was agitated

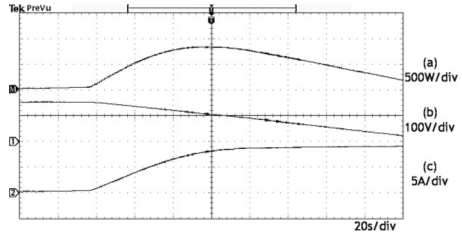

Fig. 8. Experimental results for the characteristics of solar cell array. (a) Output power. (b) Voltage of solar cell array. (c) Current of solar cell array.

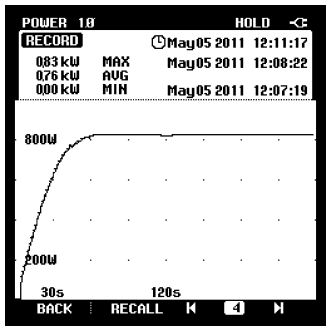

Fig. 9. Experimental results of MPPT performance for the developed photovoltaic power generation system.

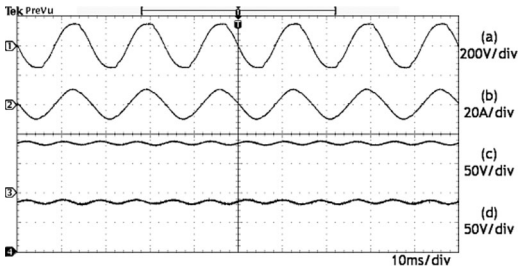

Fig. 10. Experimental results of the five-level inverter. (a) Utility voltage. (b) Output current of the five-level inverter. (c) DC capacitor voltage V_{C2}. (d) DC capacitor voltage V_{C3}.

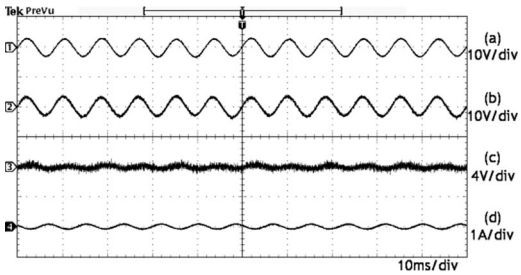

Fig. 11. Experimental results for the dc–dc converter of the developed photovoltaic power generation system. (a) Voltage ripple of dc capacitor C_2. (b) Voltage ripple of dc capacitor C_3. (c) Output voltage ripple of solar cell array. (d) Inductor current ripple of dc–dc converter.

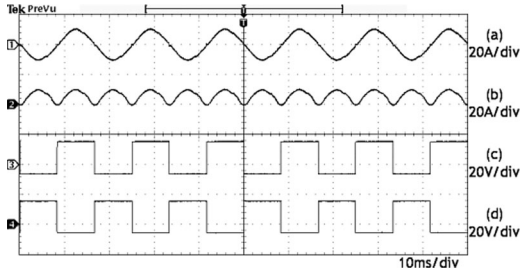

Fig. 12. Experimental results for full-bridge inverter of the five-level inverter. (a) Output current of the full-bridge inverter i_o. (b) Input current of the full-bridge inverter $i_{\rm dc}$. (c) Driver signal of S_4. (d) Driver signal of S_5.

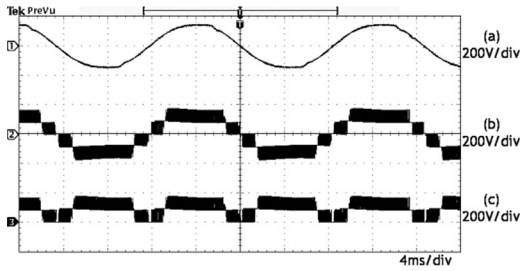

Fig. 13. Experimental results of the five-level inverter. (a) Utility voltage. (b) Output voltage of the full-bridge inverter. (c) Output voltage of the dual-buck converter.

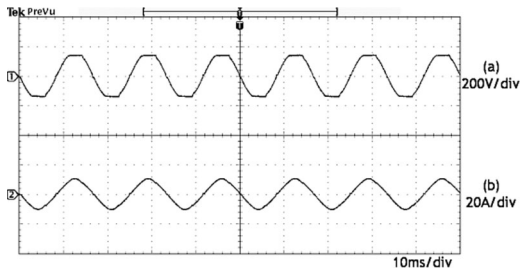

Fig. 14. Experimental results for the developed photovoltaic power generation system under the distorted utility voltage. (a) Utility Voltage. (b) Output current of the five-level inverter.

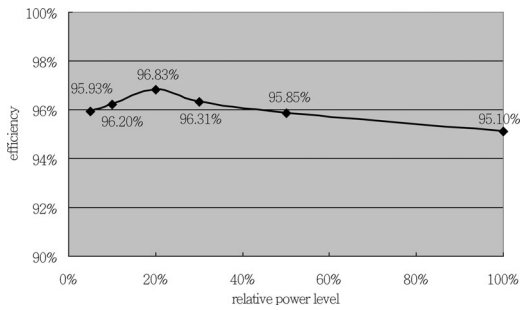

Fig. 15. Experimental results of power efficiency for the developed five-level inverter under different output power.

every 1.45 s. As seen in Fig. 9, the output power of the solar cell array in the developed photovoltaic power generation system is about 830 W. Therefore, the developed photovoltaic power generation system can track the maximum power point of the solar cell array effectively.

Fig. 10 shows the experimental results for the five-level inverter used in the developed photovoltaic power generation system under the steady state. The output power of the solar cell array is about 830 W. As seen in Fig. 10(b), the output current of the five-level inverter is sinusoidal and in phase with the utility voltage. The total harmonic distortion (THD%) of the utility voltage and the output current of the five-level inverter are 4.1% and 3.3%, respectively. As seen in Fig. 10(c) and (d), both dc capacitor voltages V_{C2} and V_{C3} remain in balance, and

TABLE III
COMPARISON OF FIVE-LEVEL INVERTERS

	diode-clamped	flying capacitor	cascade H-bridge	developed inverter
power electronics	8	8	8	6
capacitors	2	4	2	2
balancing voltages of capacitors	hard	hard	hard	easier
high-frequency switching switches	8	8	8	2

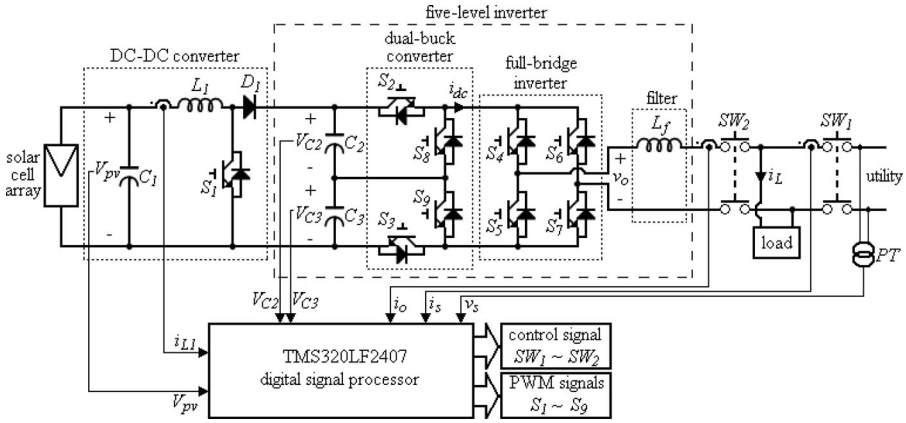

Fig. 16. Circuit configuration of the developed photovoltaic power generation system with the function of supplying reactive power.

their voltage is about 85 V, respectively. Therefore, the dc bus voltage is regulated at 170 V. This verifies the five-level inverter can perform the functions of converting solar power to ac power with unity power factor, low THD%, and balancing two dc capacitor voltages effectively.

Since dc capacitors C_2 and C_3 perform the function of energy buffers, both dc capacitor voltages V_{C2} and V_{C3} contain a 120-Hz voltage ripple. Fig. 11 shows the experimental results for the dc–dc converter of the developed photovoltaic power generation system. Fig. 11(a) and (b) show the peak-to-peak value of the voltage ripple at dc capacitors C_2 and C_3 is about 7 V. As seen in Fig. 11(c), the peak-to-peak value of the voltage ripple at the solar cell array is only about 1.6 V. Fig. 11(d) shows the ripple of the inductor current is very small due to the use of the current-mode control. In this way, the output voltage of the solar cell array can be more stable. This verifies that the developed control method for the dc–dc converter of the developed photovoltaic power generation system can effectively block the voltage ripple of five-level inverter delivering to the output voltage of the solar cell array.

Fig. 12 shows the experimental results for the full-bridge inverter of the five-level inverter. As can be seen, the input current $i_{\rm dc}$ of the full-bridge inverter shown in Fig. 12(b) is the absolute of the output current of the full-bridge inverter shown in Fig. 12(a). As seen in Fig. 12(c) and (d), the switch frequency of the power electronic switches S_4 and S_5 is 60 Hz. This verifies the power electronic switches of the full-bridge inverter are switched in low frequency, and the full-bridge inverter can convert the dc power into ac power by commutating.

Fig. 13 shows the experimental voltage of the five-level inverter. As seen in Fig. 13(c), the dual-buck converter outputs a dc voltage with three levels $V_{\rm dc}$, $V_{\rm dc}$/2, and 0. Fig. 13(b) shows the output voltage of the dual-buck converter is further converted to an ac voltage with five voltage levels $V_{\rm dc}$, $V_{\rm dc}$/2, 0, $-V_{\rm dc}$/2, and $-V_{\rm dc}$ by the full-bridge inverter. The voltage variation of each level is $V_{\rm dc}$/2. This verified that the five-level inverter can generate a five-level output ac voltage according to the utility voltage and only the power electronic switches of the dual-buck converter is switched in high frequency.

Fig. 14 shows the experimental results for the developed photovoltaic power generation system under the distorted utility voltage. As seen in Fig. 14(a), the utility voltage is distorted, and its THD% is 8.4%. As seen in Fig. 14(b), the output current of the five-level inverter is still close to sinusoidal, and its THD% is only 4.5% and the power factor is 0.99. This experiment verifies the controller of the five-level inverter can control the output current with low THD% even when the utility voltage is distorted.

Fig. 15 shows the experimental results of power efficiency for the developed five-level inverter under different output power. The solar cell array was replaced by a dc power supply in this experiment, and the dc power supply is connected the dc bus so as to simplify the adjustment output power of five-level inverter in the experimental process. As seen in Fig. 15, the power efficiency is 95.10% at full load and the maximum efficiency is 96.83%. Besides, the European efficiency of the five-level inverter is 95.90%.

Table III shows the comparison of the developed five-level inverter with the conventional five-level inverters (diode-clamped, flying capacitor, and cascade H-bridge). As seen in Table III, the developed five-level inverter is superior to the conventional five-level inverters.

In IEEE Std. 929-2000 [25], the displace power factor of the small capacity inverter must be higher than 0.85. In the IEC

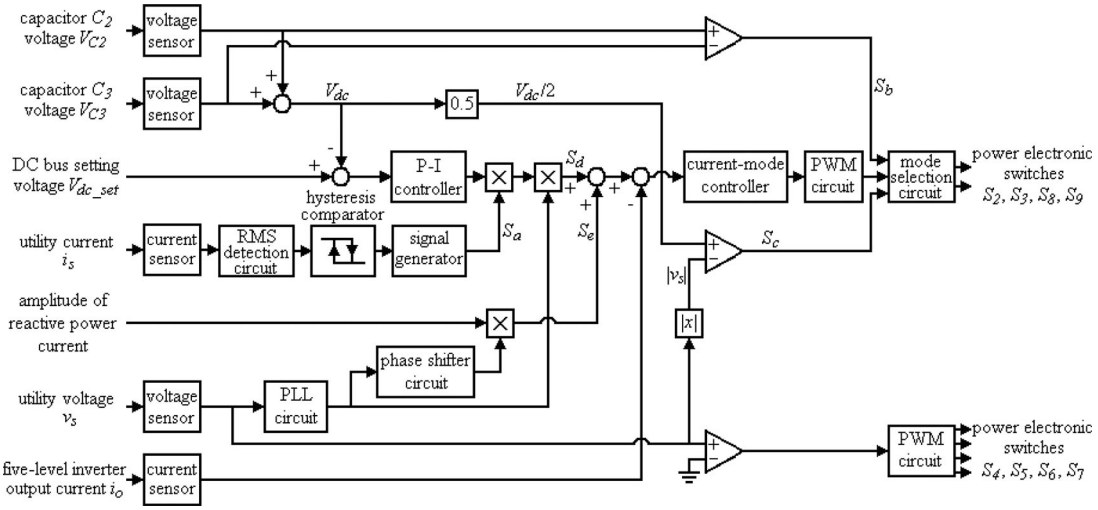

Fig. 17. Control block diagram of five-level inverter with the function of supplying reactive power.

62109-2 standard [26], the displace power factor must be higher than 0.95 and the reactive power is not required to be controlled if the dc–ac inverter capacity is smaller than 3.68 kVA. Since the capacity of the prototype in this paper is 1.2 kW, the dc–ac inverter generates ac power with the unity power factor is acceptable. If the five-level inverter must supply reactive power to the utility, two power electronic switches must replace the diodes D_2 and D_3. So, the circuit configuration of the developed photovoltaic power generation system shown in Fig. 2 must be changed to Fig. 16. Besides, a reactive power control loop must be added in the control circuit of five-level inverter shown in Fig. 6. Therefore, the control block diagram of five-level inverter must be changed to Fig. 17.

The switching operations of the replaced power electronic switches are complementary to those of power electronic switches S_2 and S_3, respectively. Accordingly, the five-level inverter can supply active power and reactive power simultaneously.

VII. Conclusion

A photovoltaic power generation system with a five-level inverter is developed in this paper. The five-level inverter can perform the functions of regulating the dc bus voltage, converting solar power to ac power with sinusoidal current and in phase with the utility voltage, balancing the two dc capacitor voltages, and detecting islanding operation. The experimental results verify the developed photovoltaic power generation system, and the five-level inverter achieves the expected performance.

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